AMENDMENTS TO THE SPECIFICATION

Please replace the last fully paragraph at page 2 with the following amended paragraph:

In the via first type dual damascene structure, first and second insulating ~~layers~~ interlayers are sequentially formed. Then, a via hole is formed in the first insulating interlayer, and then, a groove is formed in the second insulating interlayer. Finally, a via structure and a groove wiring layer are simultaneously formed in the via hole and the groove, respectively.

Please replace the paragraph bridging pages 2 and 3 with the following amended paragraph:

In the middle first type dual-damascene structure, a first insulating interlayer is formed, and a via hole etching mask is formed on the first insulating interlayer. Then, a second insulating ~~inter layer~~ interlayer is formed. Then, a groove is formed in the second insulating interlayer simultaneously with the formation of a via hole in the first insulating interlayer using the via hole as an etching mask. Finally, a via structure and a groove wiring layer are simultaneously formed in the via hole and the groove, respectively. In the middle first type dual-damascene structure, note that anti-reflective layers for suppressing reflective light from an under Cu layer cannot be used in the photolithography processes for the formation of the via hole mask and the groove.

Please replace the second full paragraph at page 10 with the following amended paragraph:

First, referring to Fig. 2A, an insulating underlayer 201 made of silicon dioxide or the like is formed on a silicon substrate (not shown) where various semiconductor elements are formed. Then, an etching stopper 202 made of SiN is formed by a plasma CVD process on the insulating underlayer 201. Then, an insulating interlayer 203 made of silicon dioxide is deposited by a CVD process on the etching stopper 202. Then, an anti-reflective coating layer 204 and a photoresist layer 205 are sequentially coated on the insulating interlayer 203. Then, the photoresist layer 205 is patterned by a photolithography process, so that a groove 205a is formed in the photoresist layer 205.

Please replace the last full paragraph at page 13 with the following amended paragraph:

In the method as illustrated in Figs. 2A through 2P, when the copper diffusion barrier layer 208 is overetched, the copper layer 207 is oxidized by the dry ashing process using O2 gas plasma, which decreases the manufacturing yield of the via structure and enhances the electromignation of the via structure. If the ~~photolightography~~ photolithography and etching process for the insulating interlayers 211 and 209 fails, photolithography and etching processes for the insulating interlayers 211 and 209 are repeated. In this case, since the copper layer 207 is further oxidized by the dry ashing process using O2 gas plasma, the manufacturing yield of the via structure is further decreased as shown in Fig. 3. This is true for a middle-first type dual-damascene structure and a trench-first type dual-damascene structure.

Please replace the paragraph nos. 17-19 at page 29 **with the following amended paragraph:**

First, referring to Fig. 10A, an insulating underlayer 201 made of silicon dioxide or the like is formed on a silicon substrate (not shown) where various semiconductor elements are formed. Then, an about 50 nm thick etching stopper 202 made of SiCN is formed by a plasma CVD process on the insulating underlayer 201. Then, an about 300nm thick insulating interlayer 203a made of a low-k material such as SiOF, SiOC, organic material or inorganic material such as ladder-type hydrogen siloxane having a lower dielectric constant than that of silicon dioxide is coated on the etching stopper 202. Then, an about 100nm thick mask insulating layer 203b made of silicon dioxide is deposited by a plasma CVD process on the insulating interlayer 203a. Then, an anti-reflective coating layer 204 and a photoresist layer 205 are sequentially coated on the mask insulating layer 203b. Then, the photoresist layer 205 is patterned by a photolithography process, so that a groove 205a is formed in the photoresist layer 205.

Please replace the first fully paragraph at page 34 with the following amended paragraph:

Next, referring to Fig. 10N, the mask insulating layer 211b, the insulating interlayer 211a and the etching stopper 210 are etched by a dry etching process using CF based gas plasma and using the photoresist layer 215 as a mask.